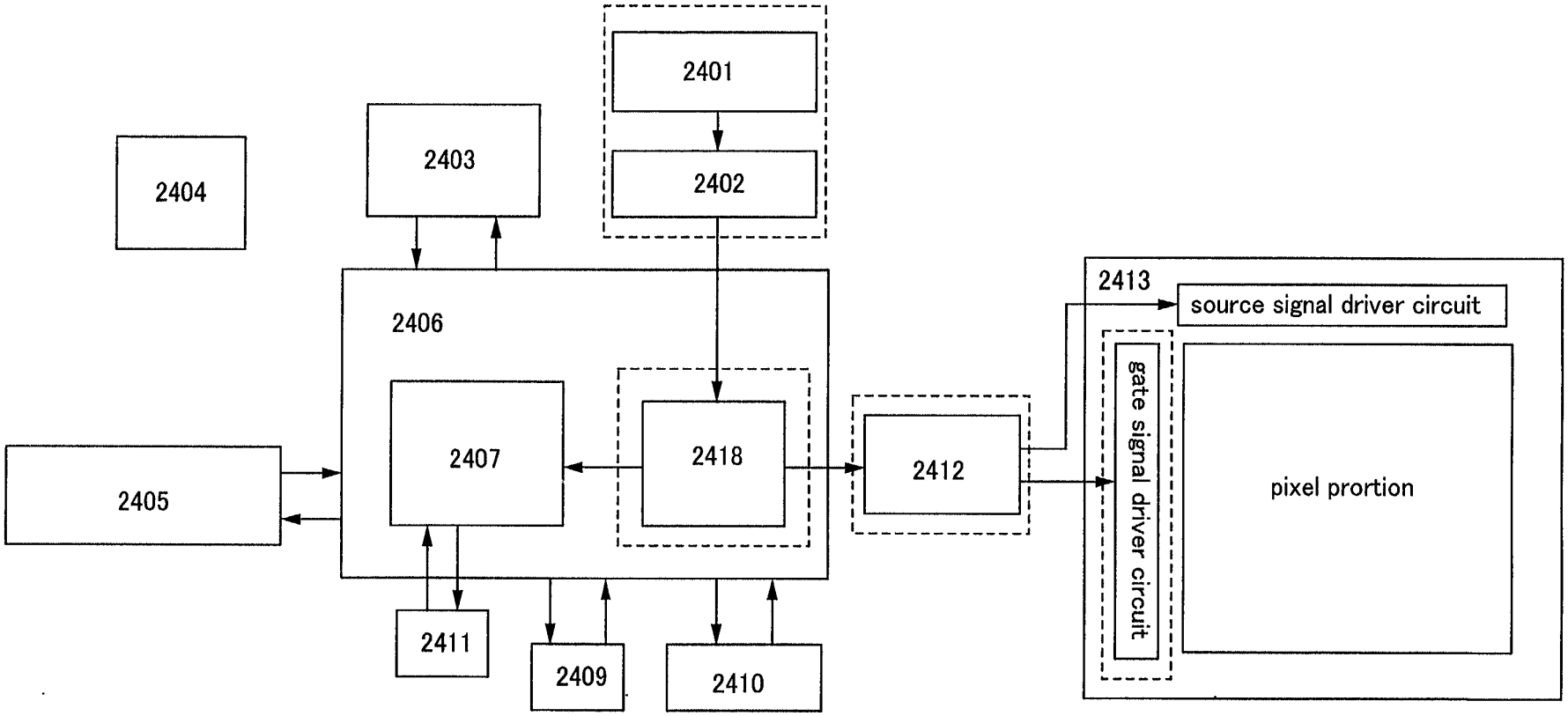


Fig. 1

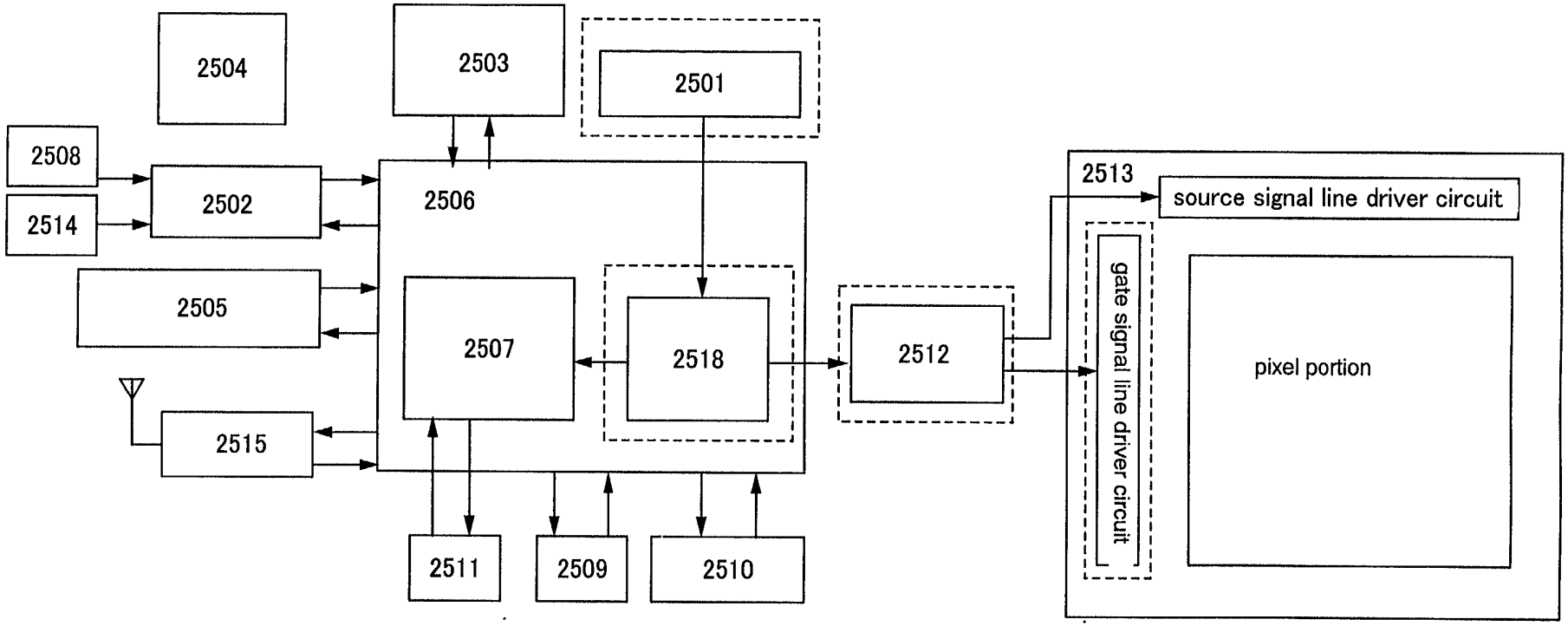


Fig. 2

Fig. 3A

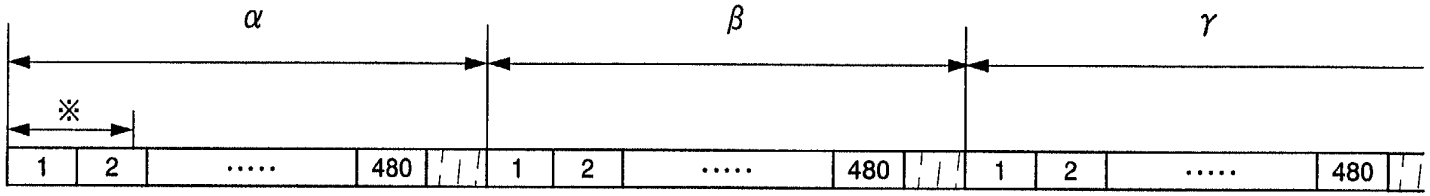
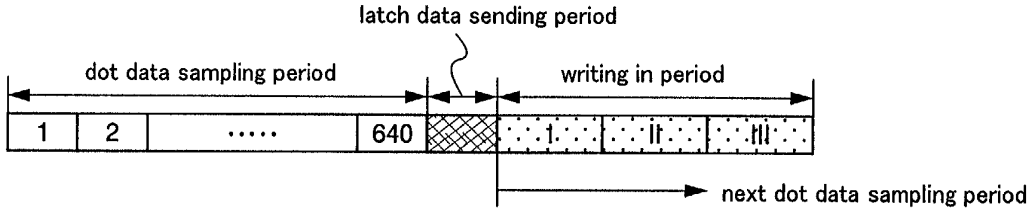

α
β
γ
※
1
2
.....
480
1
2
.....
480
1
2
.....
480

Fig. 3B


latch data sending period
dot data sampling period
writing in period
1
2
.....
640
I
II
III
next dot data sampling period

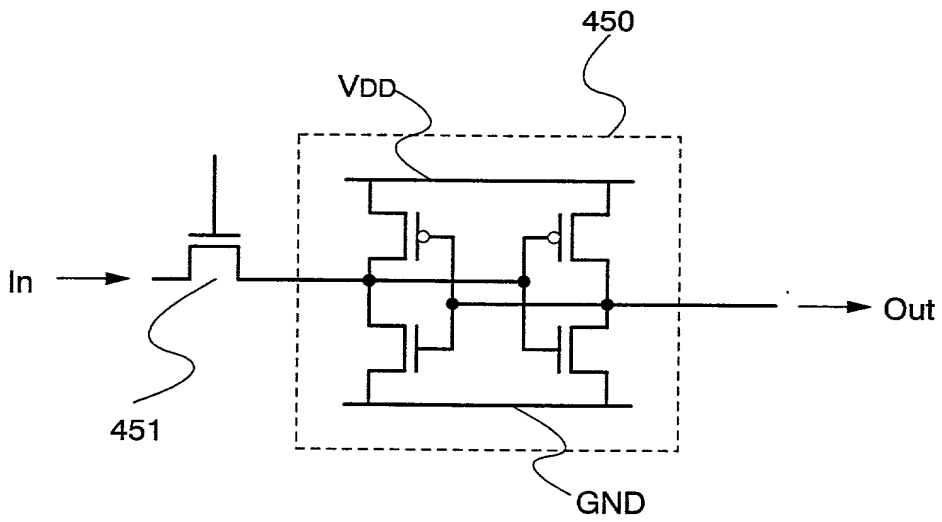


Fig. 4

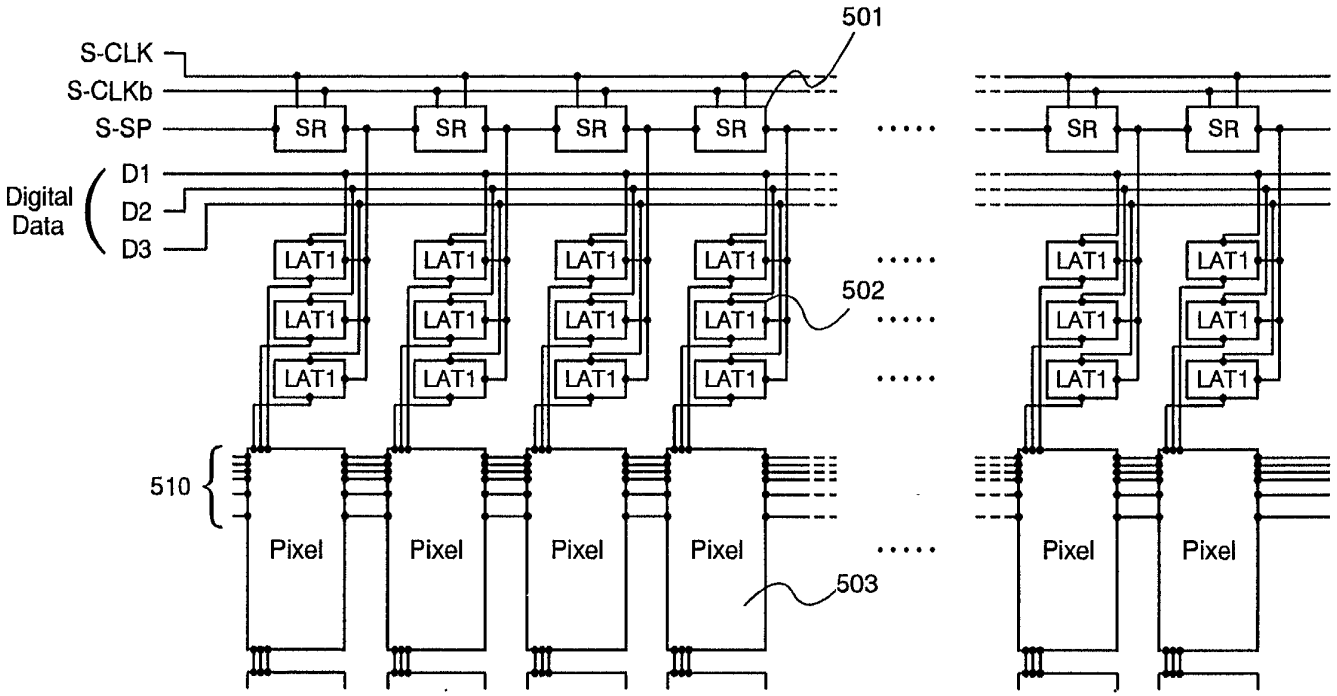


Fig. 5

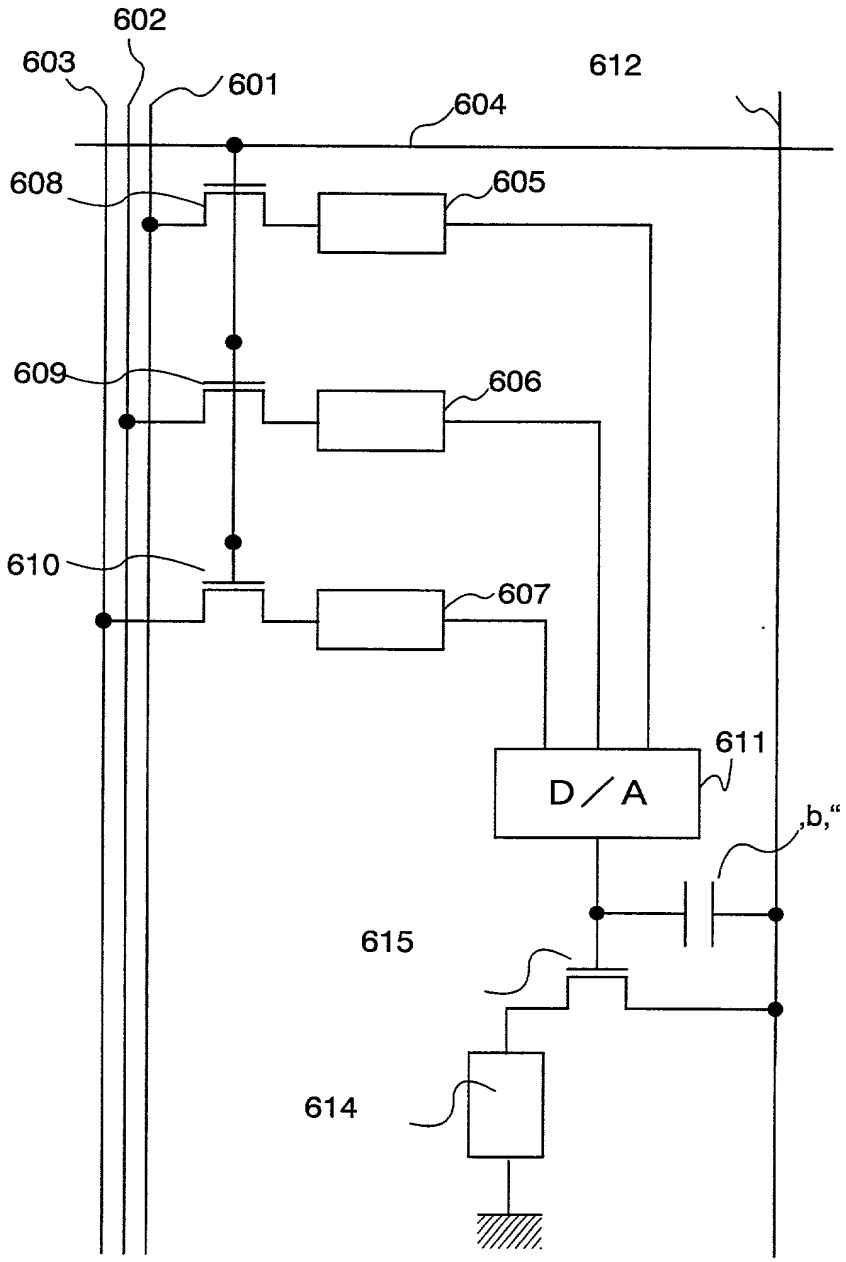


Fig. 6

Fig. 7A

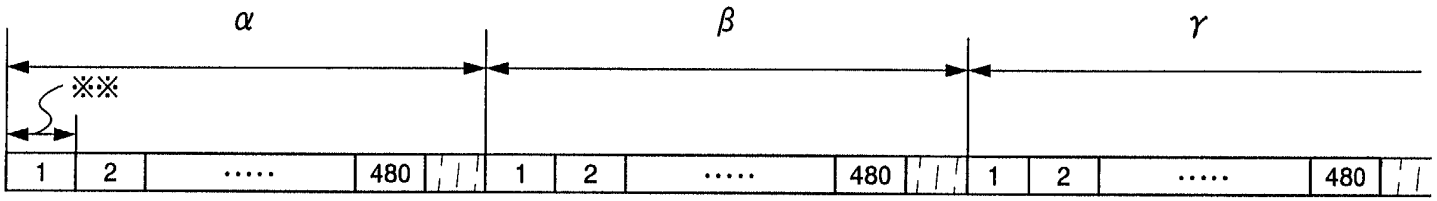
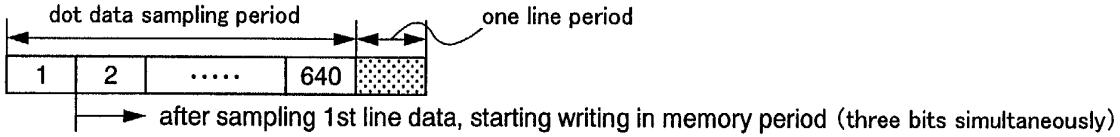

α
β
γ
※※
1
2
.....
480
1
2
.....
480
1
2
.....
480

Fig. 7B


dot data sampling period
one line period
1
2
.....
640
after sampling 1st line data, starting writing in memory period (three bits simultaneously)

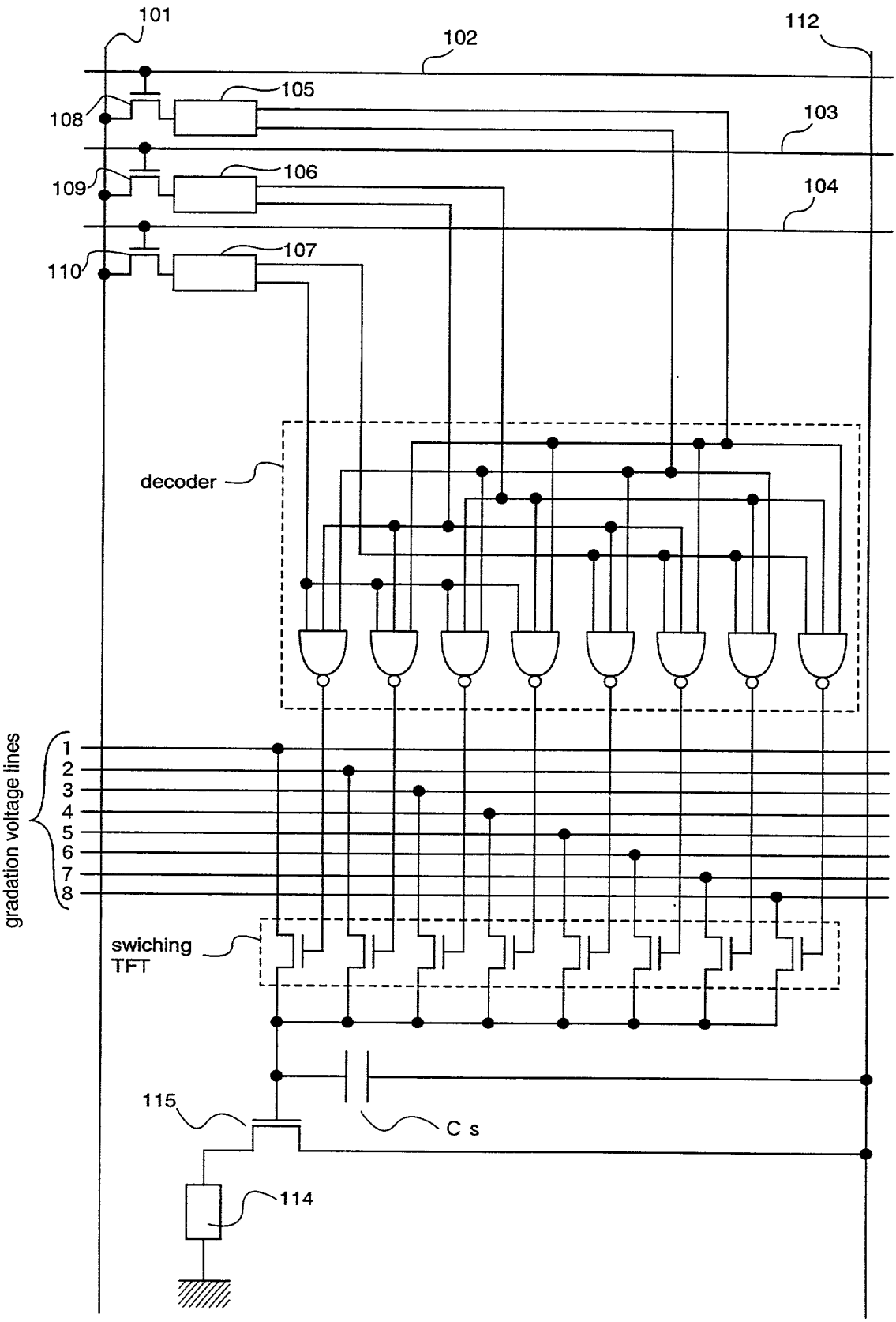

101
102
112
105
108
103
106
109
104
107
110
decoder
gradation voltage lines
1
2
3
4
5
6
7
8
swiching
TFT
115
C s
114

Fig. 8

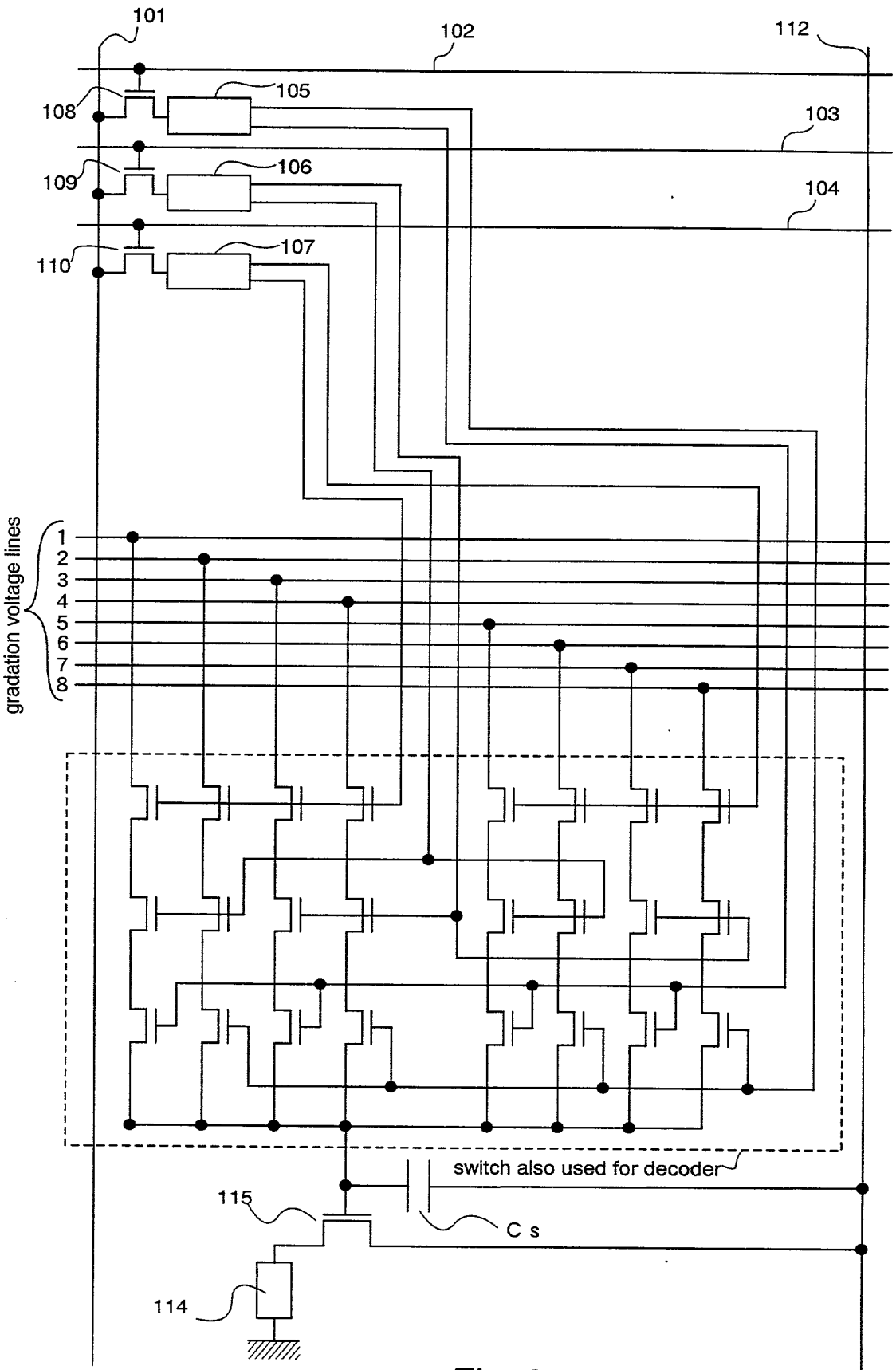

101
102
112
105
108
103
106
109
104
107
110
gradation voltage lines
1
2
3
4
5
6
7
8
switch also used for decoder
115
C s
114

Fig. 9

Fig. 10A

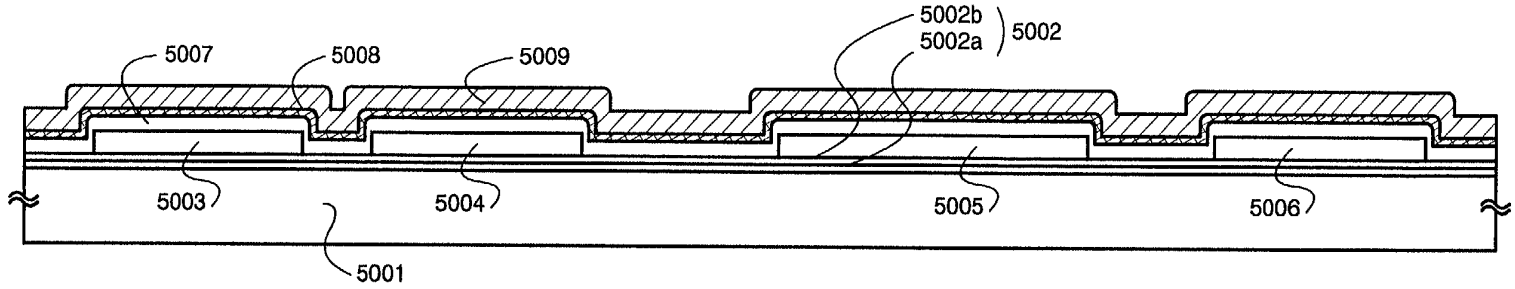


Fig. 10B

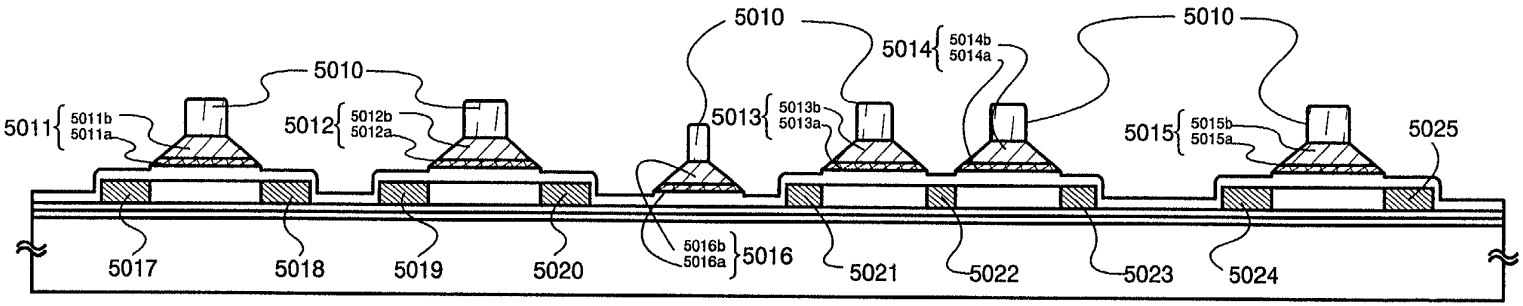


Fig. 10C

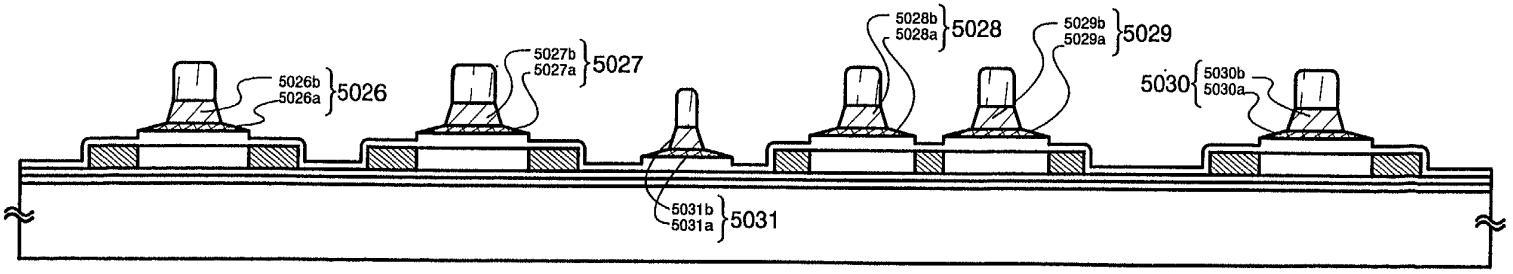


Fig. 11A

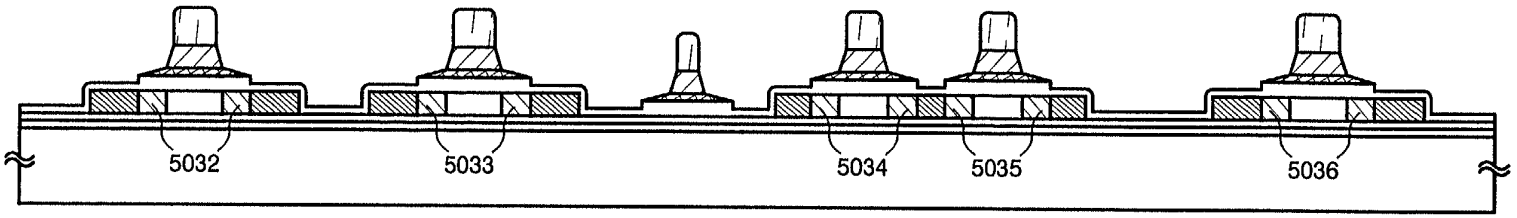


Fig. 11B

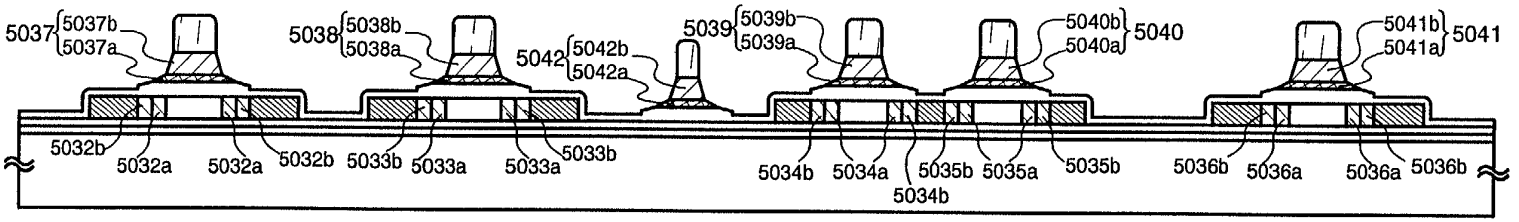


Fig. 11C

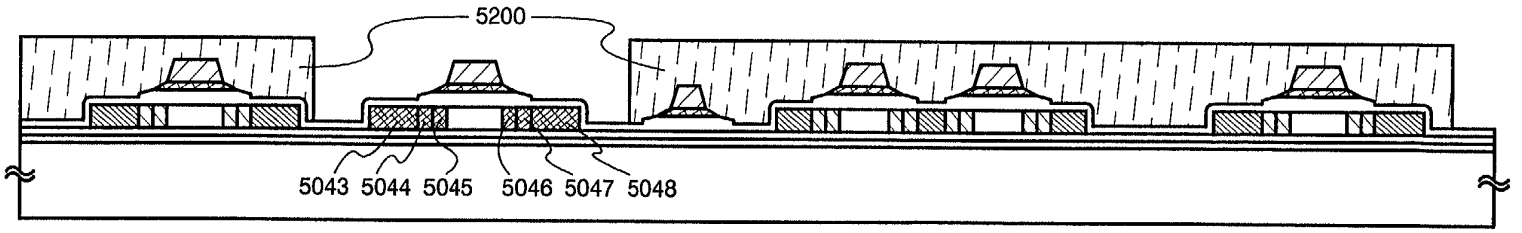


Fig. 12A

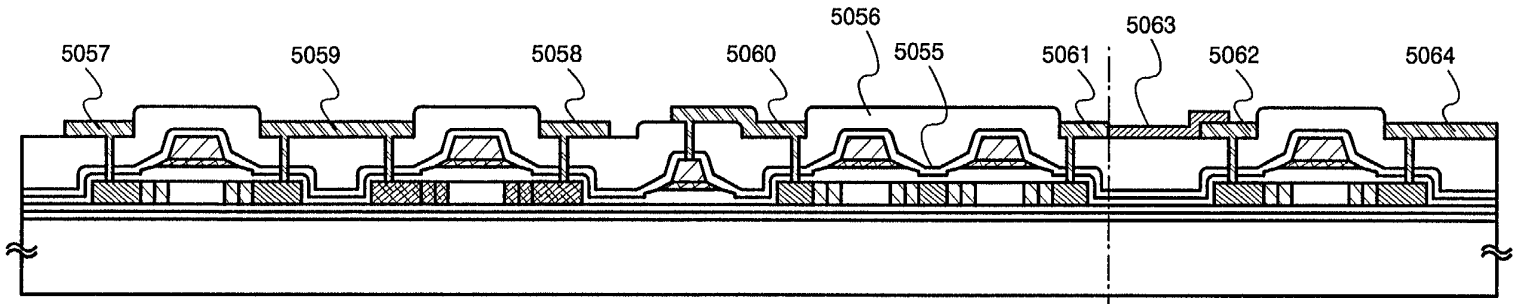
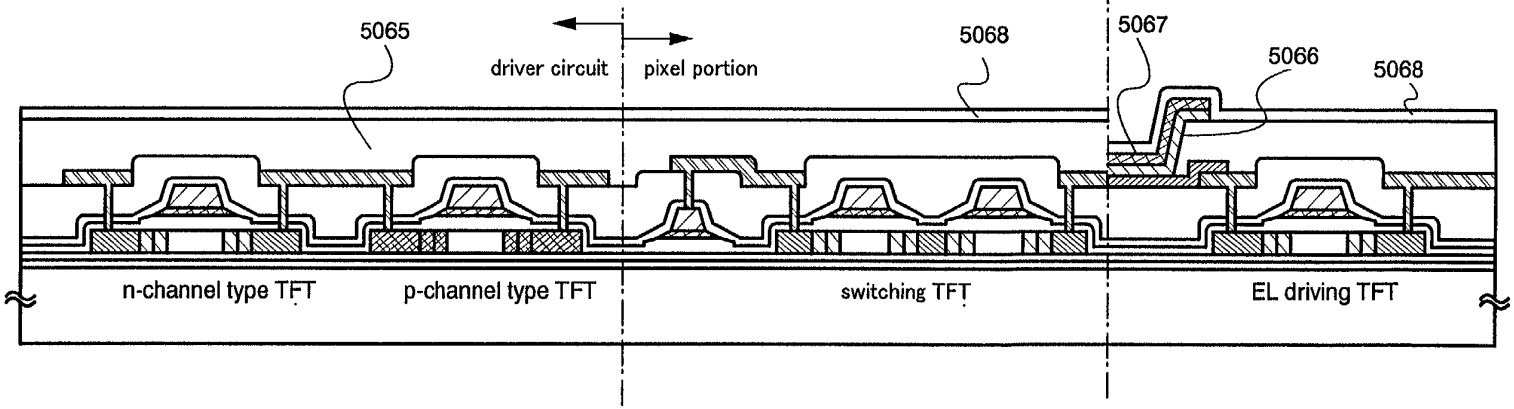


Fig. 12B



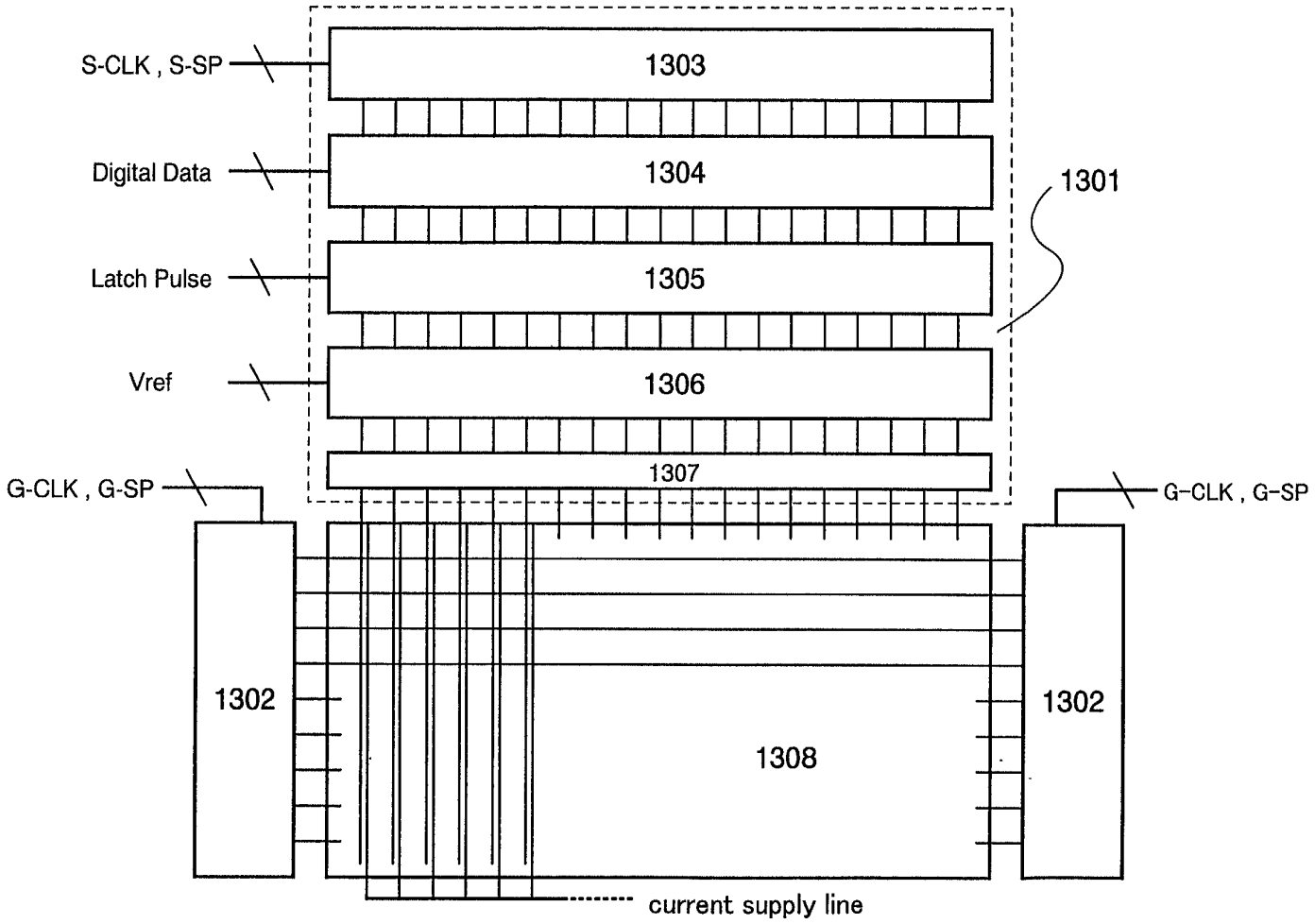


Fig. 13

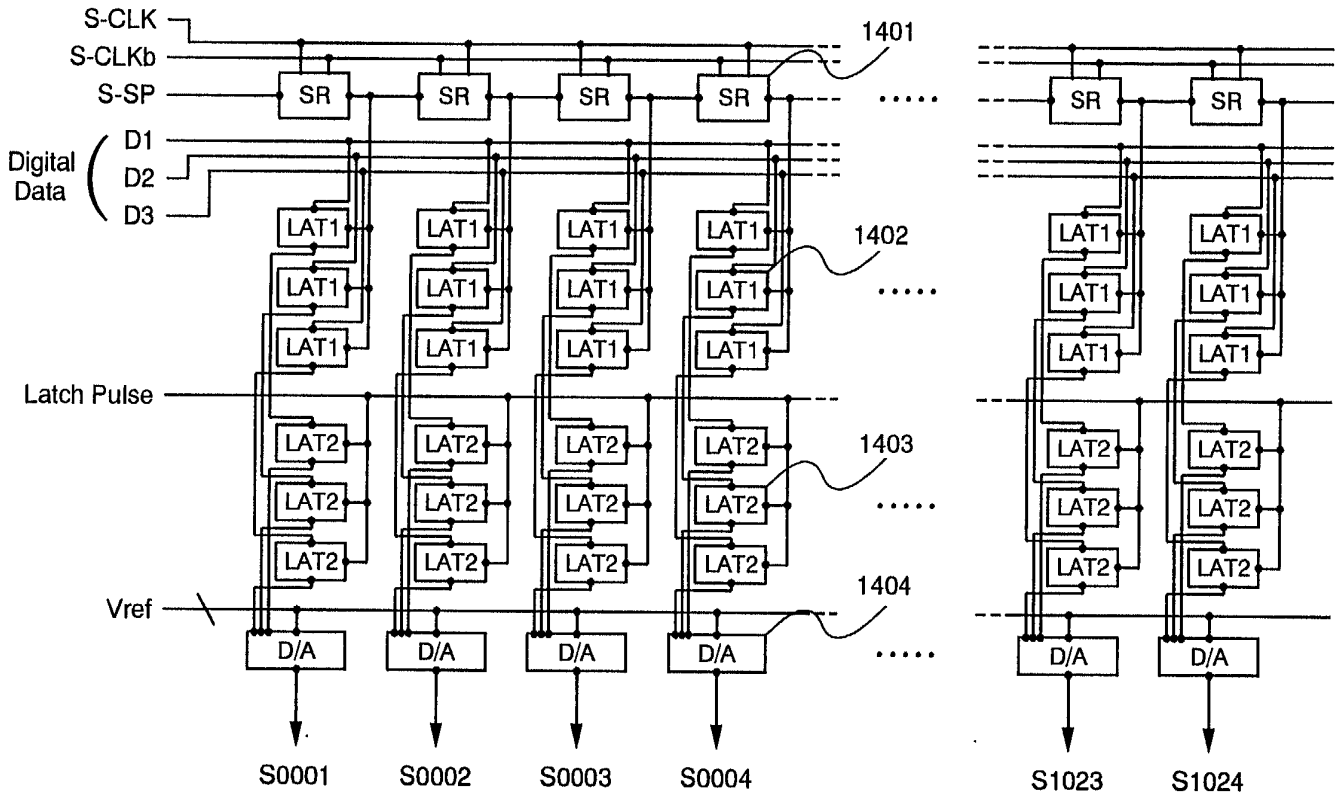


Fig. 14

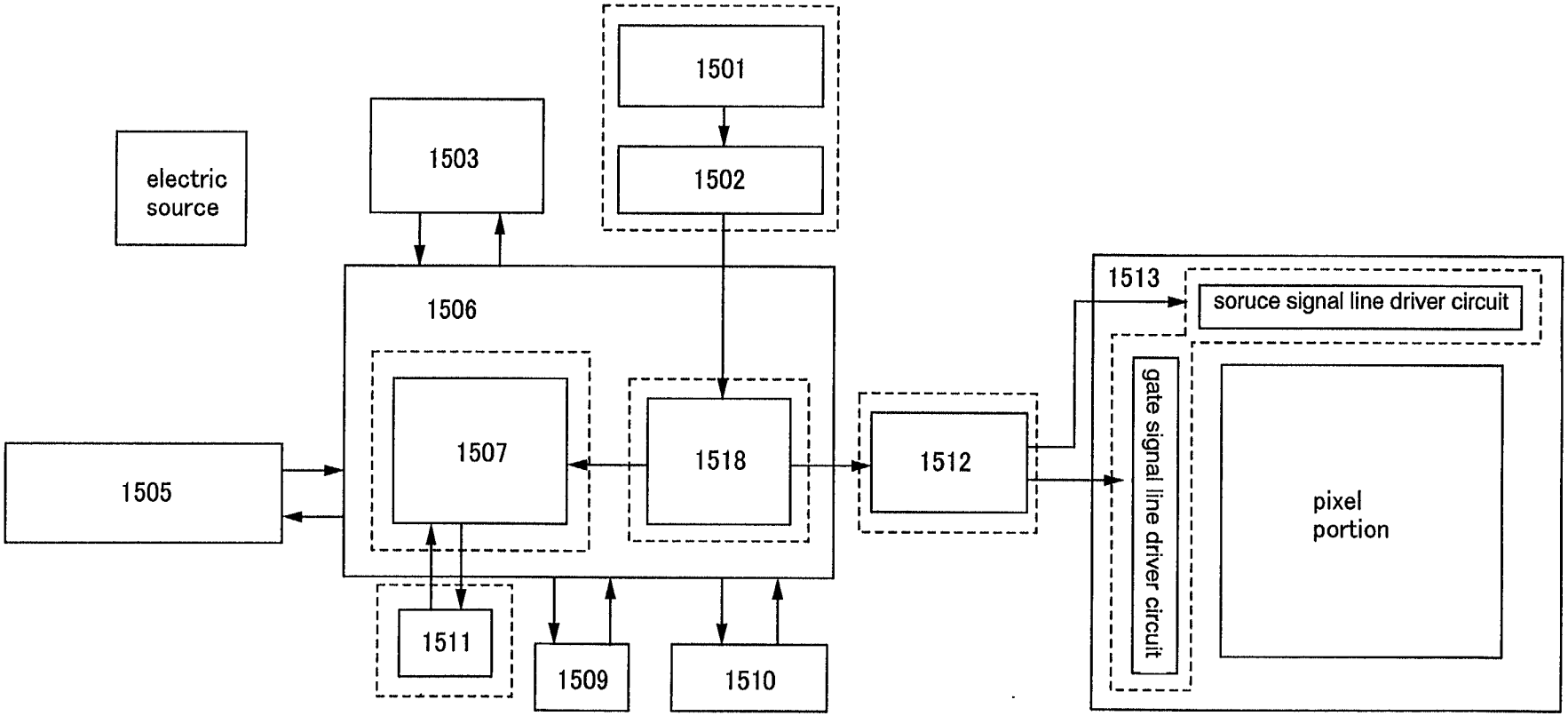


Fig. 15

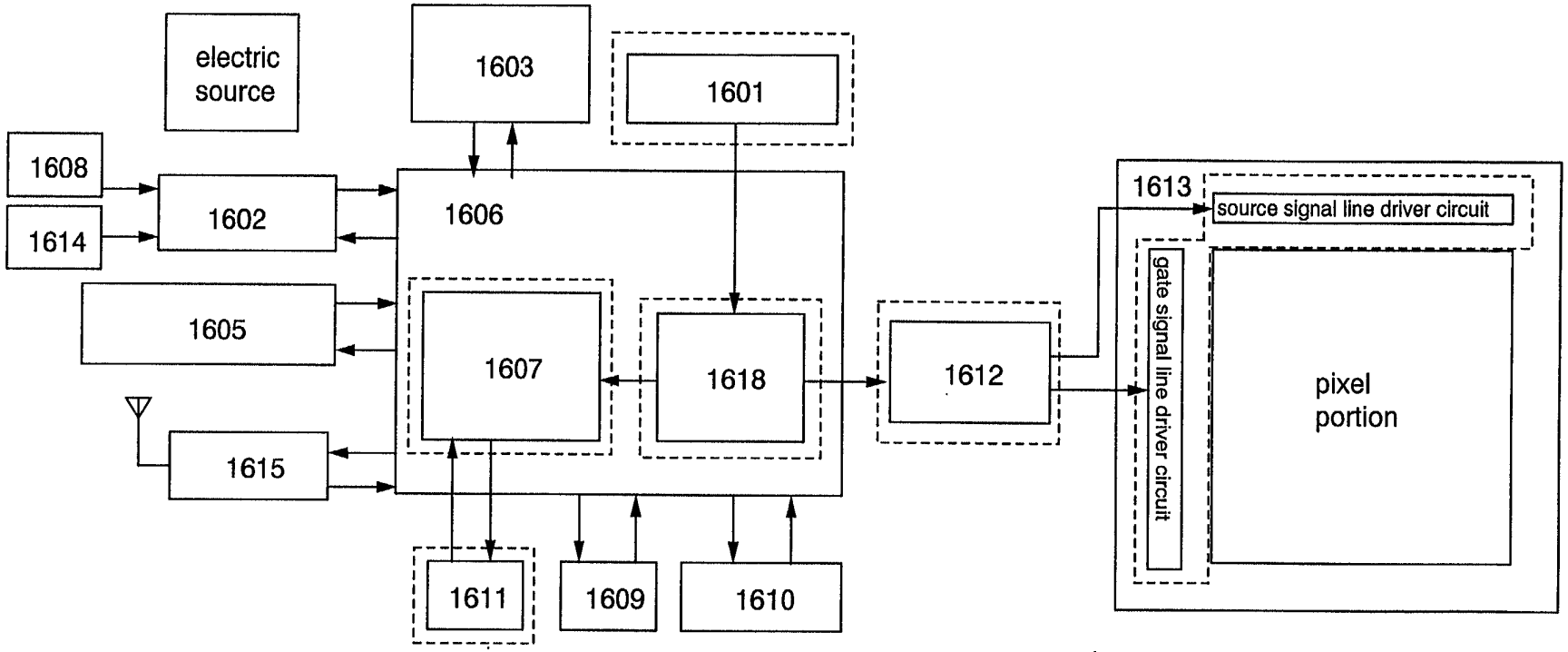


Fig. 16

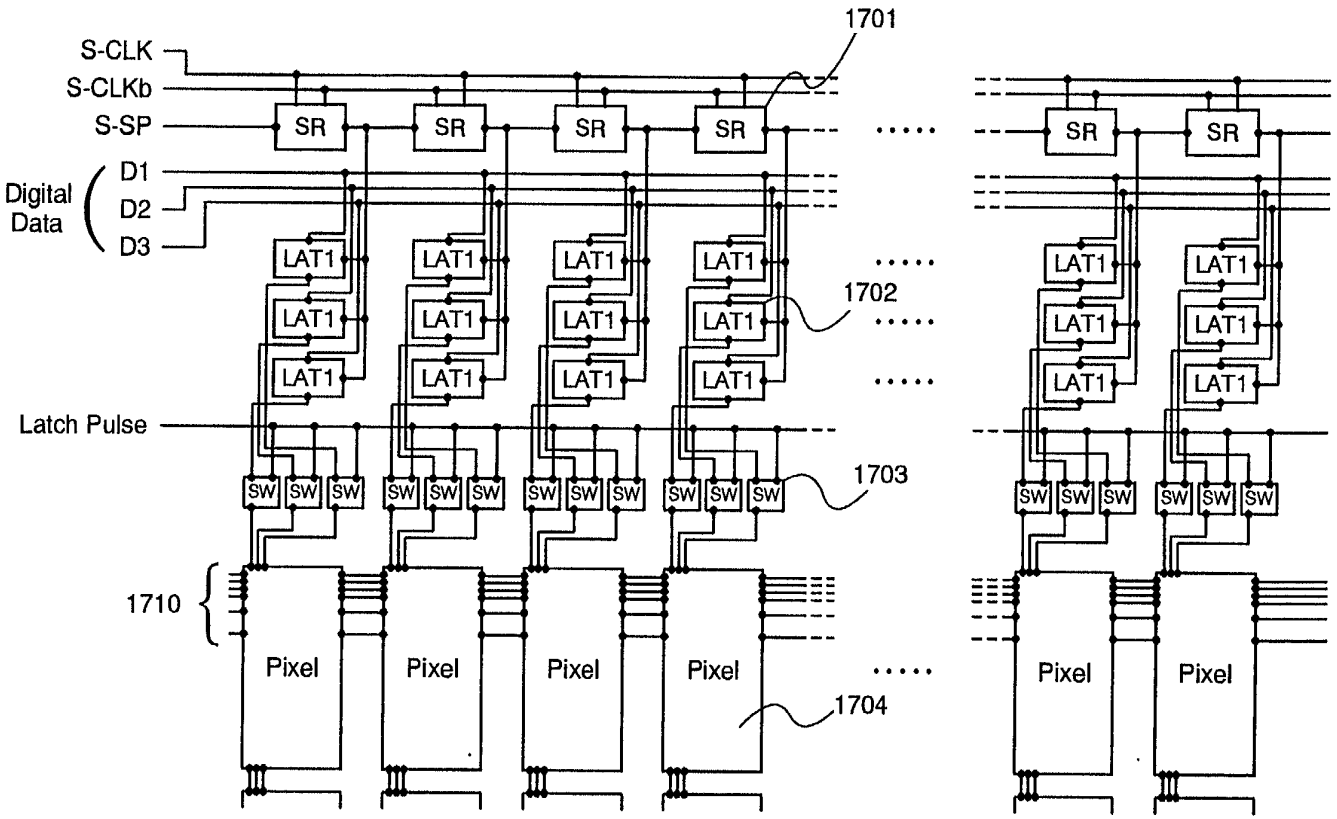


Fig. 17

Fig. 18A

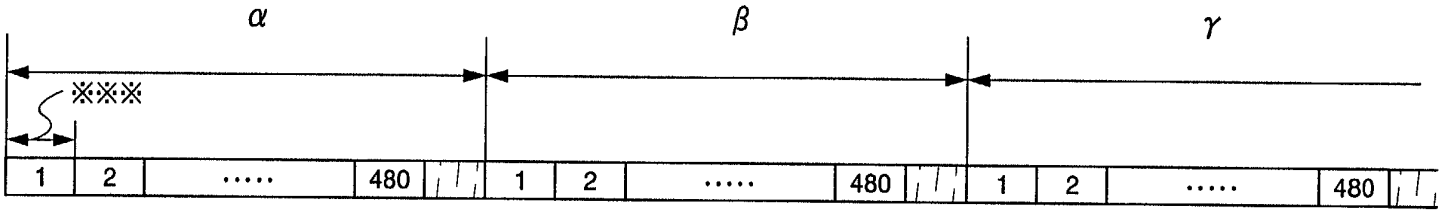


Fig. 18B

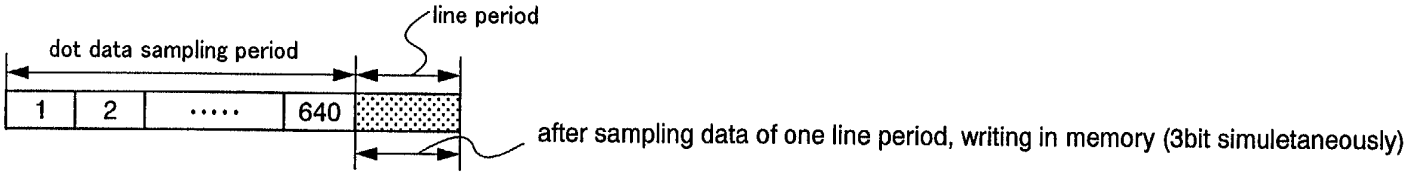


Fig. 19A

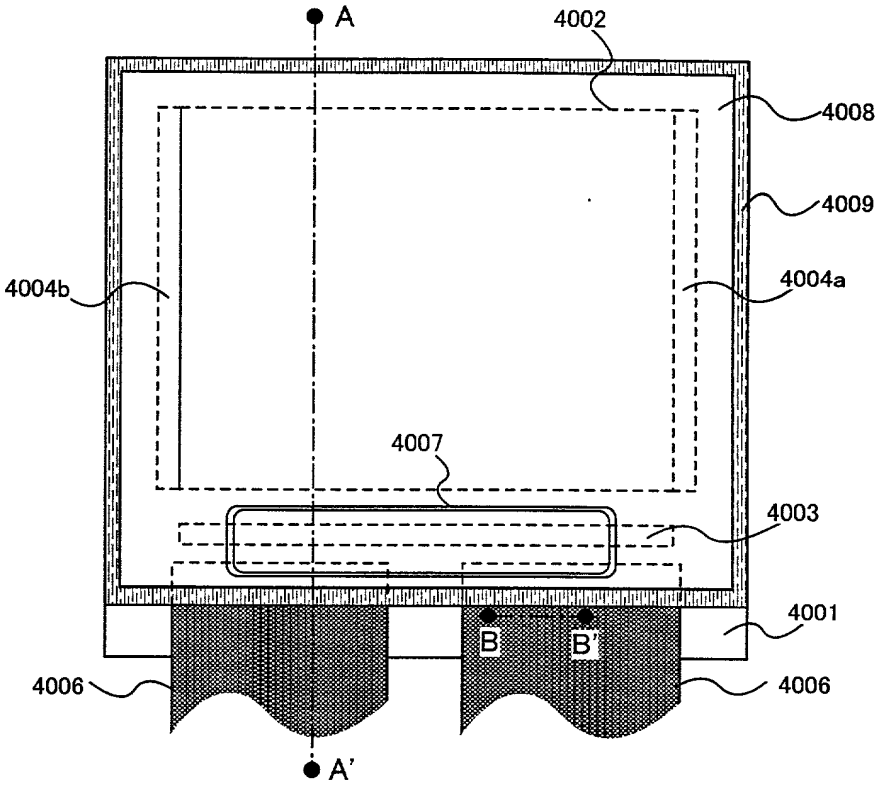


Fig. 19B

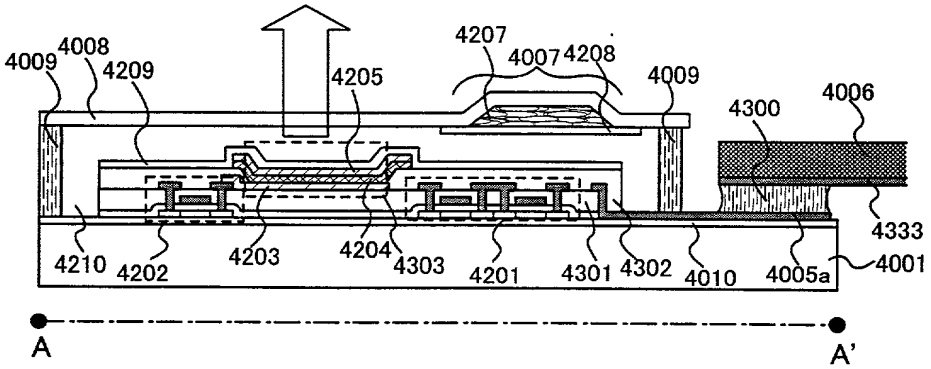
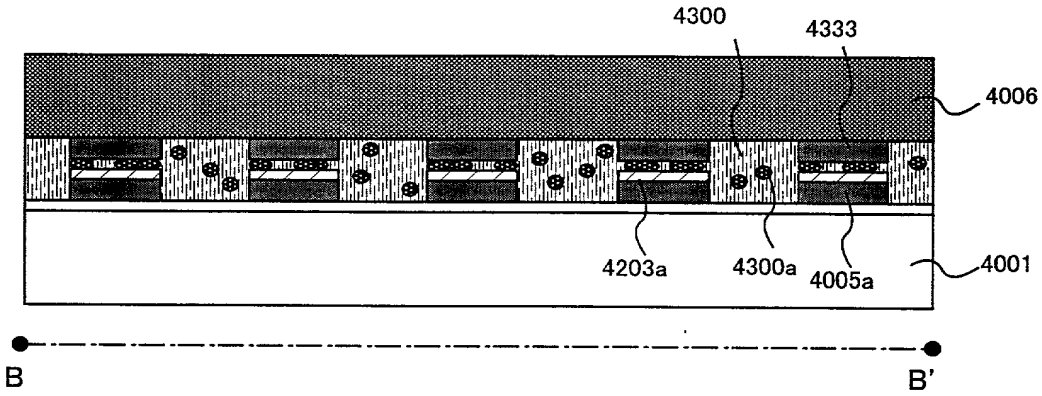


Fig. 19C



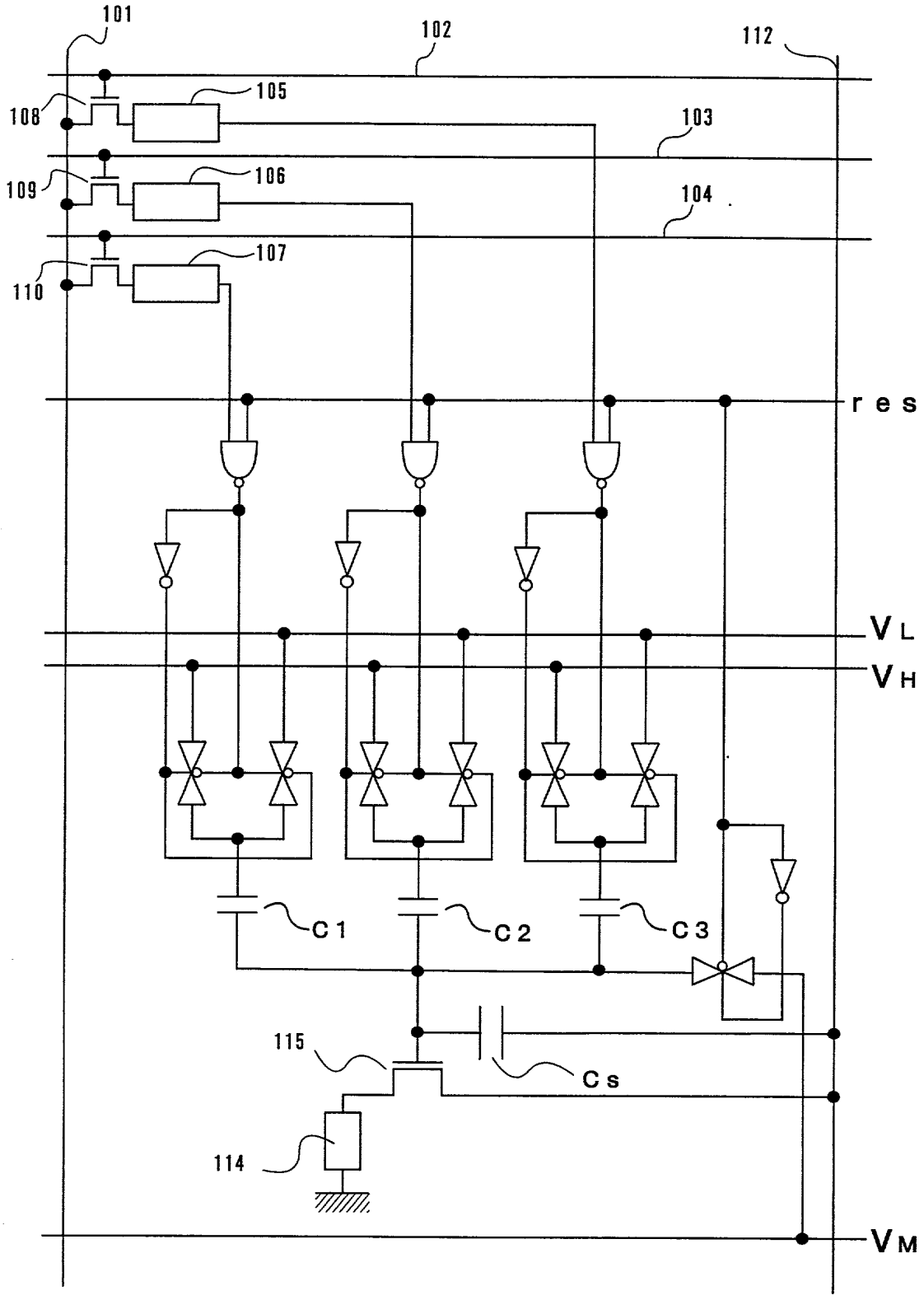

101
102
112
105
108
103
106
109
104
107
110
res
VL
VH
C1
C2
C3
115
Cs
114
VM

Fig. 20

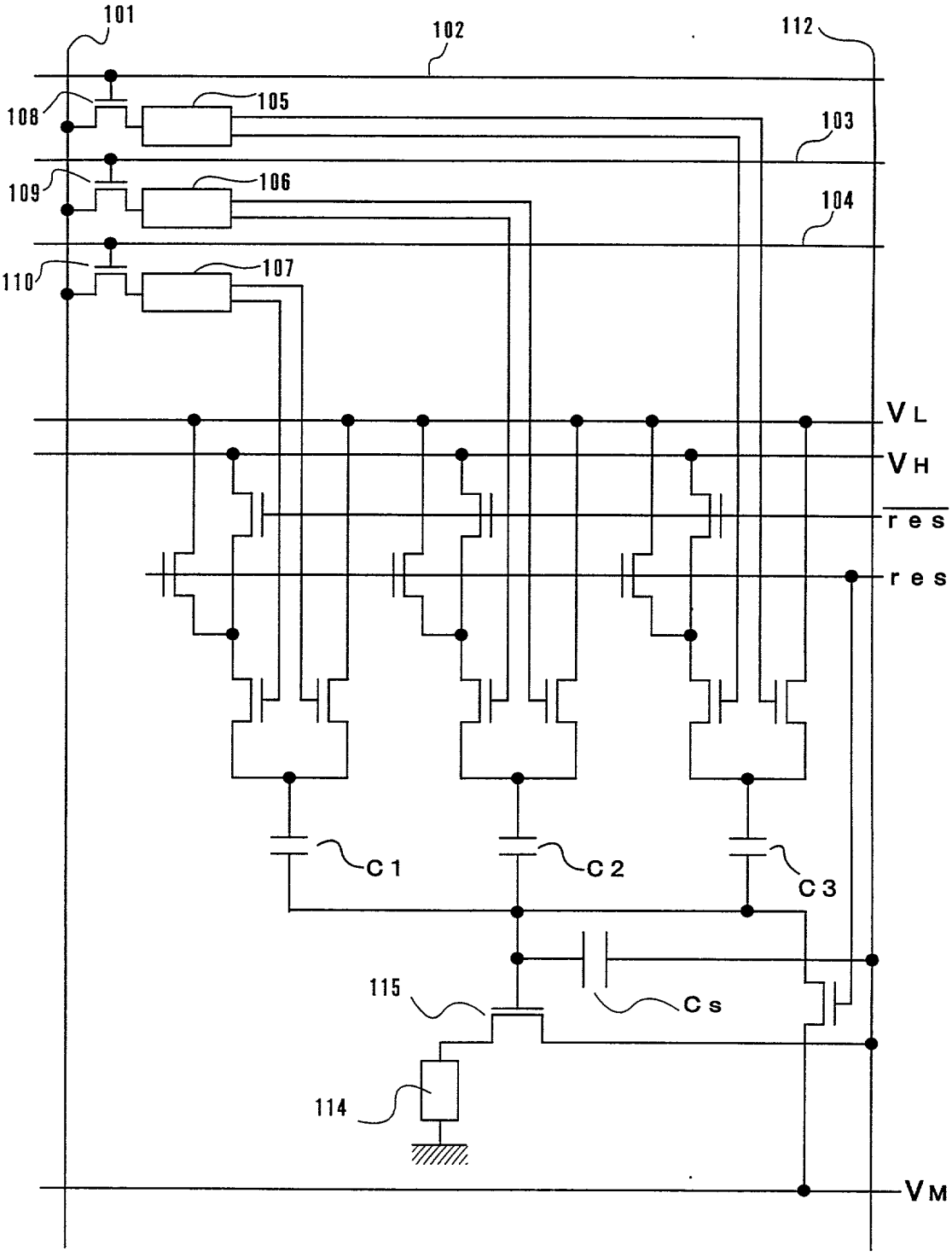

101
102
112
108
105
103
109
106
104
110
107
VL
VH
res
res
C1
C2
C3
115
Cs
114
VM

Fig. 21

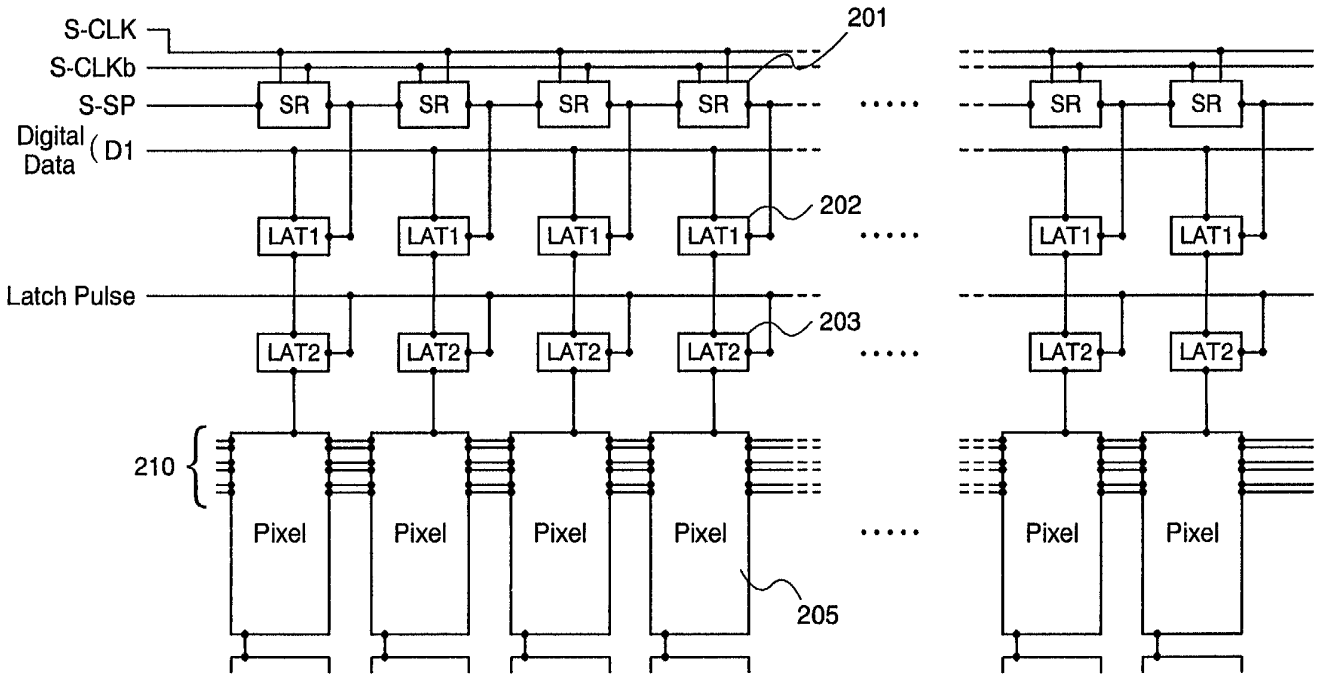

S-CLK
S-CLKb
S-SP
Digital Data
D1
Latch Pulse
SR
LAT1
LAT2
Pixel
201
202
203
205
210

Fig. 22

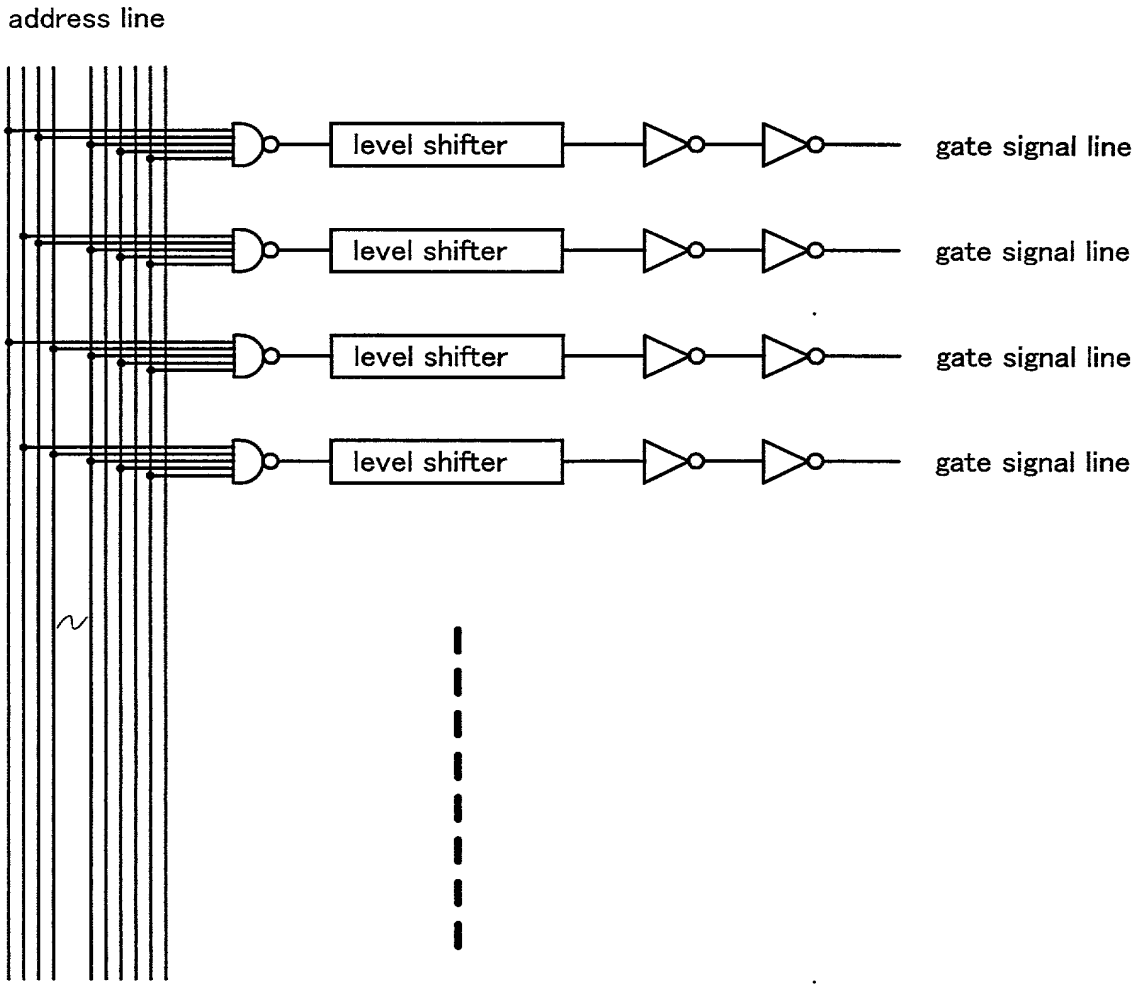

address line
level shifter
level shifter
level shifter
level shifter
gate signal line
gate signal line
gate signal line
gate signal line

Fig. 23

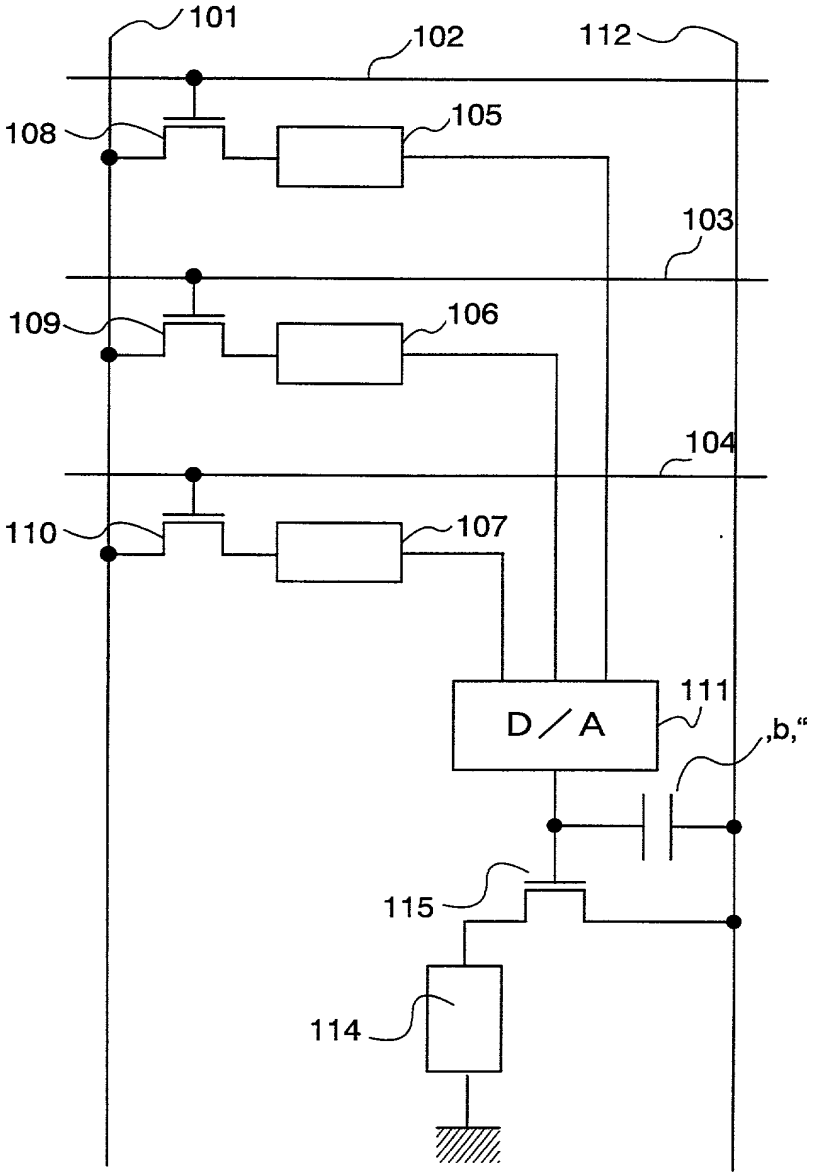


Fig. 24

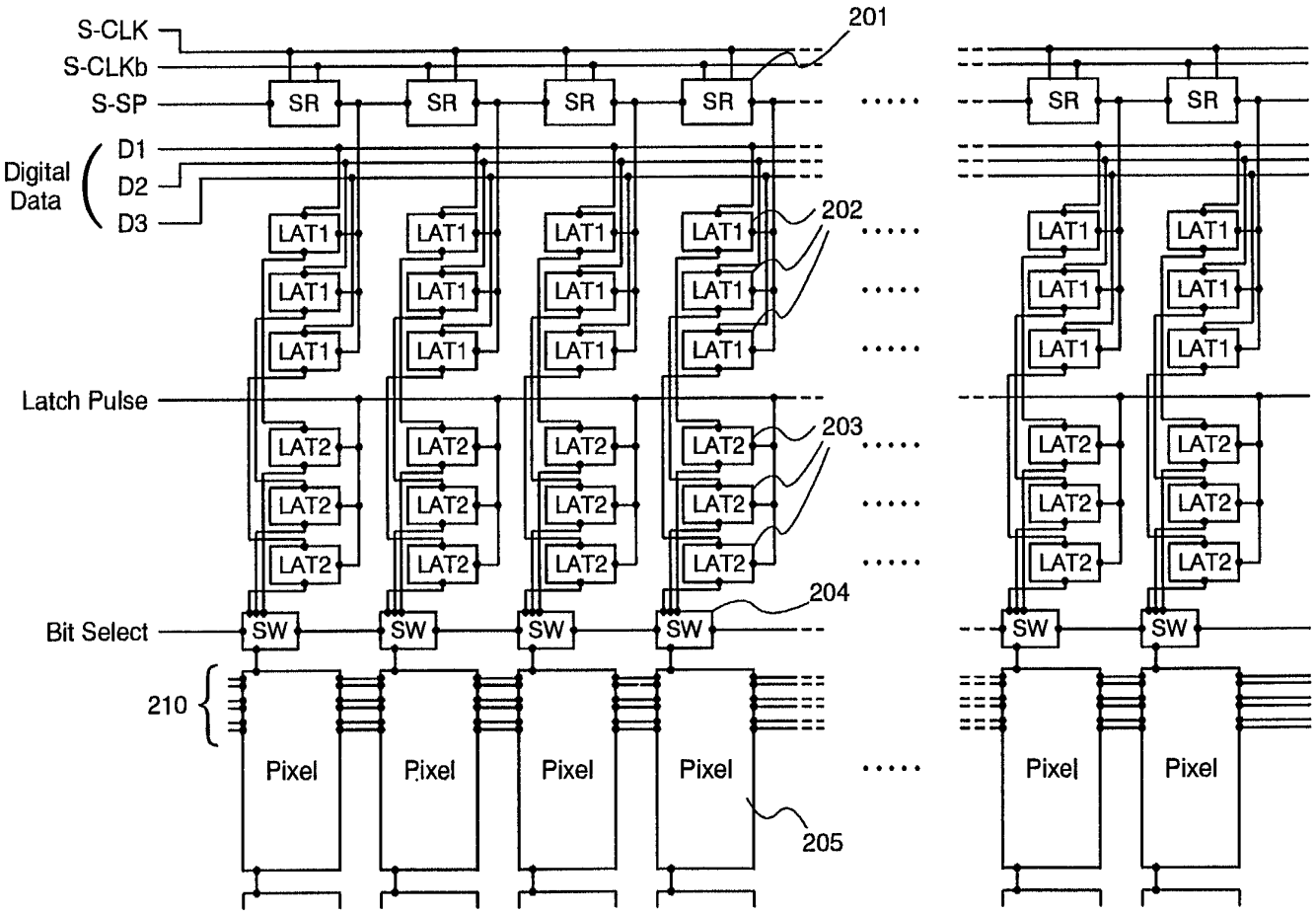


Fig. 25

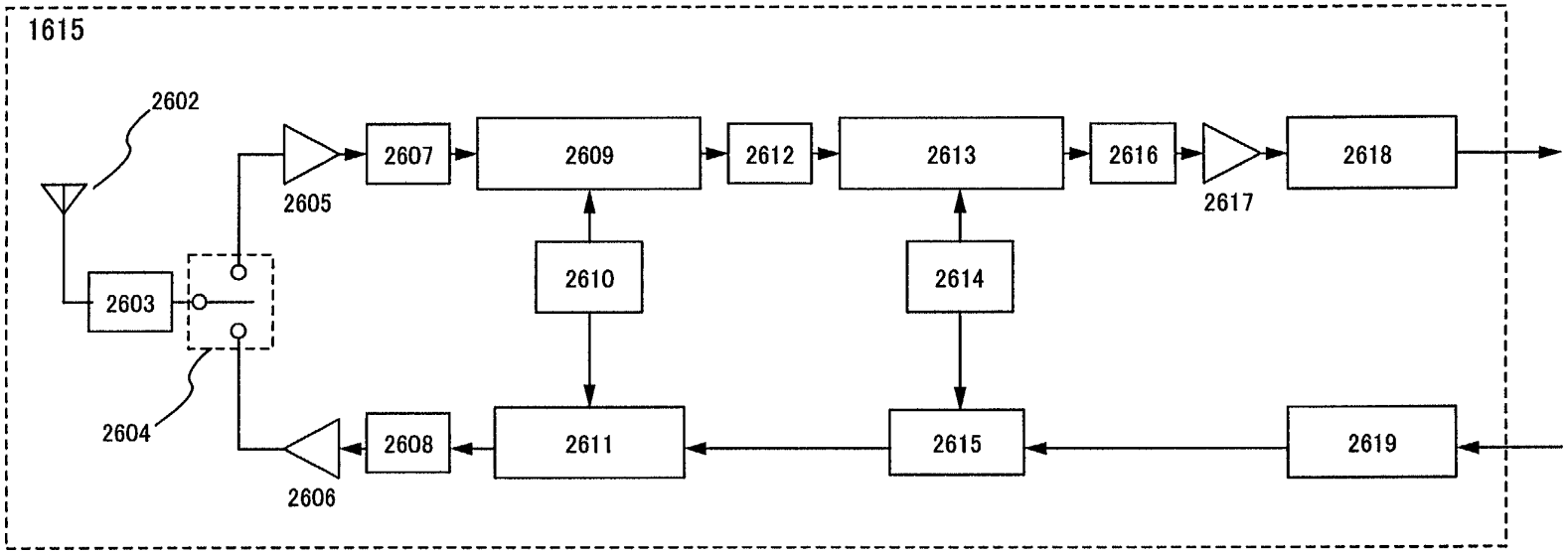


Fig. 26

Fig. 27A

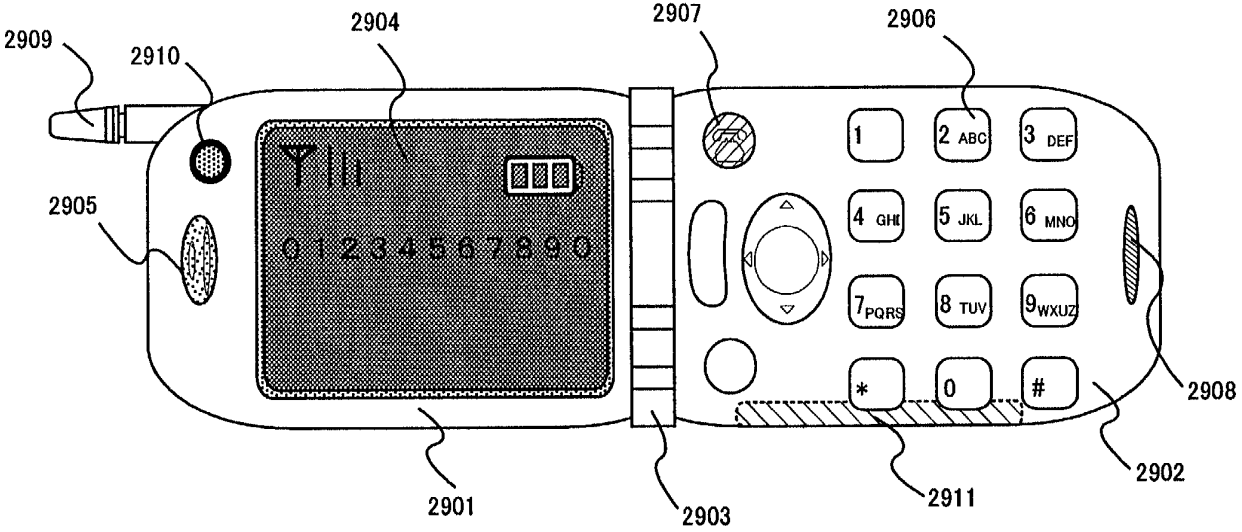
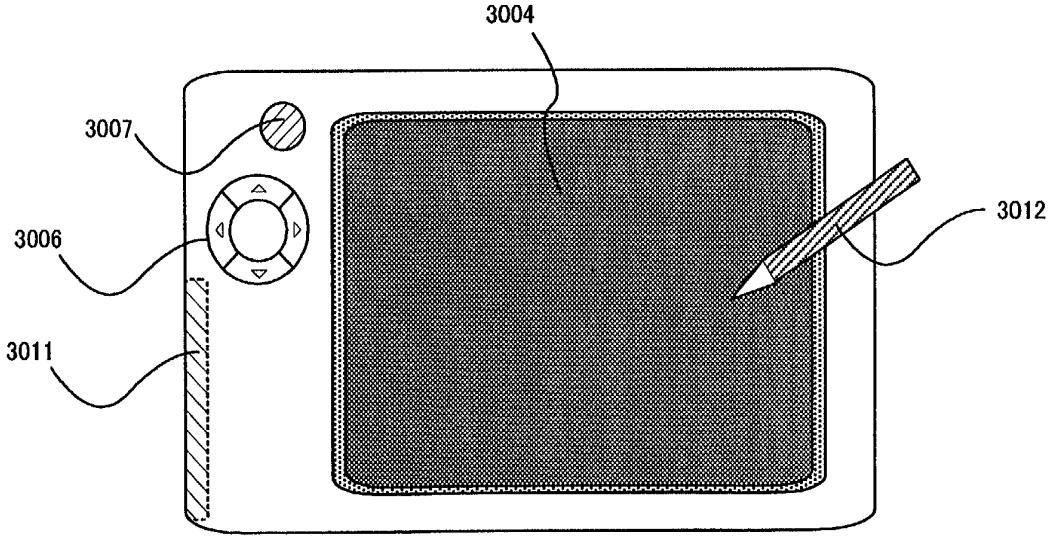


Fig. 27B



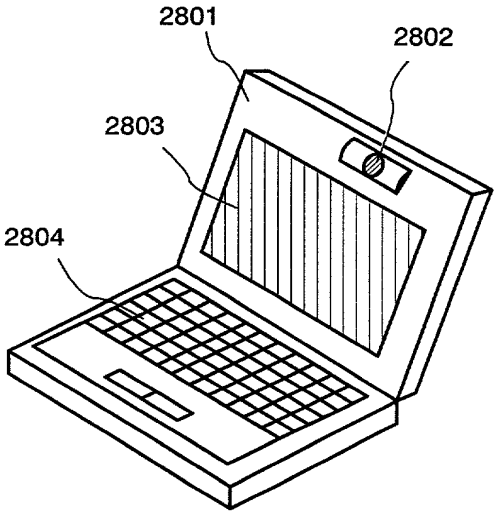


Fig. 28A

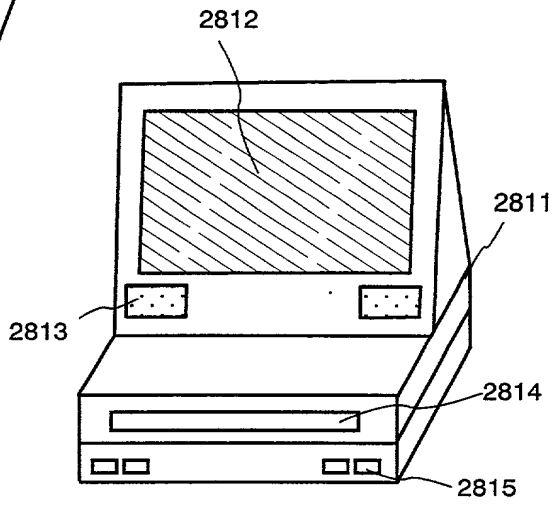


Fig. 28B

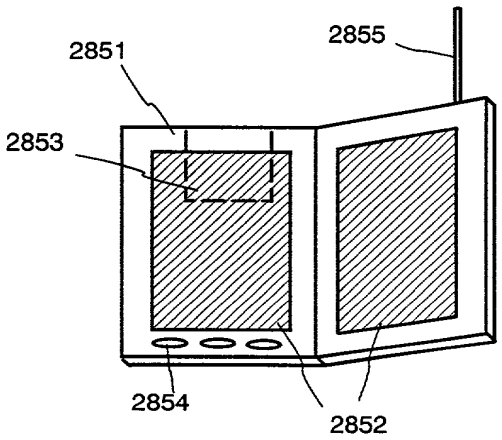


Fig. 28C

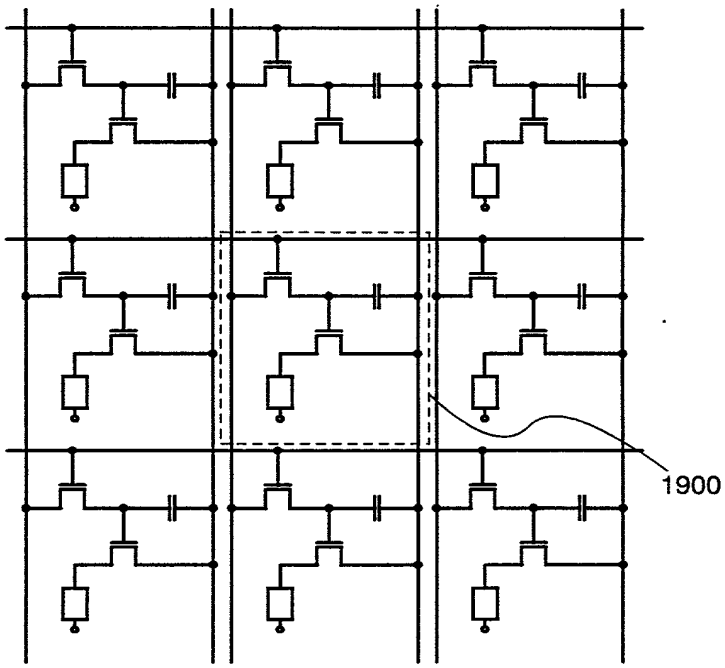


Fig. 29A

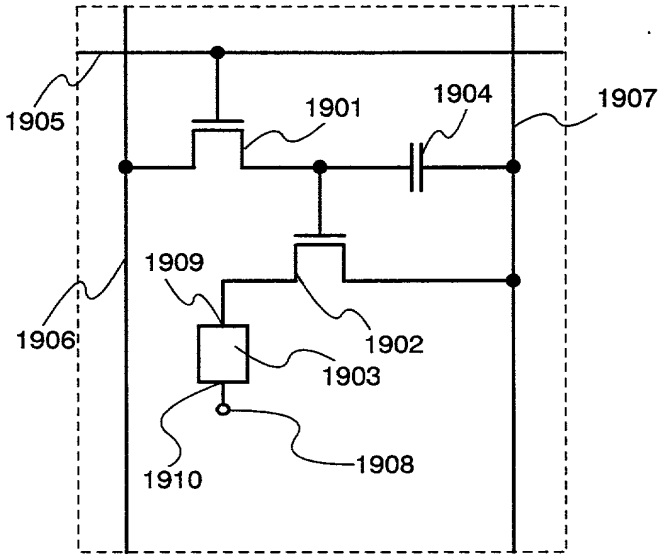


Fig. 29B

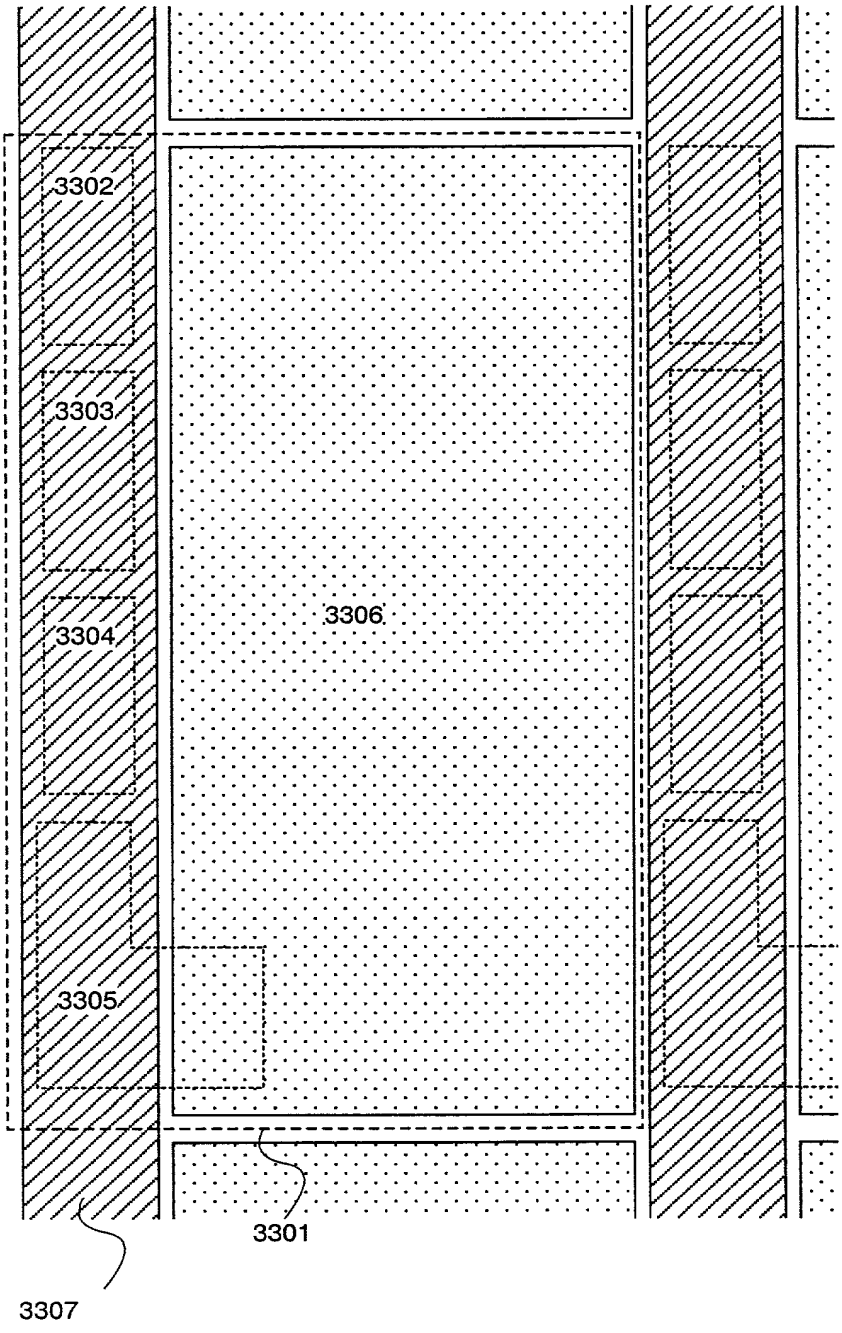


Fig. 30

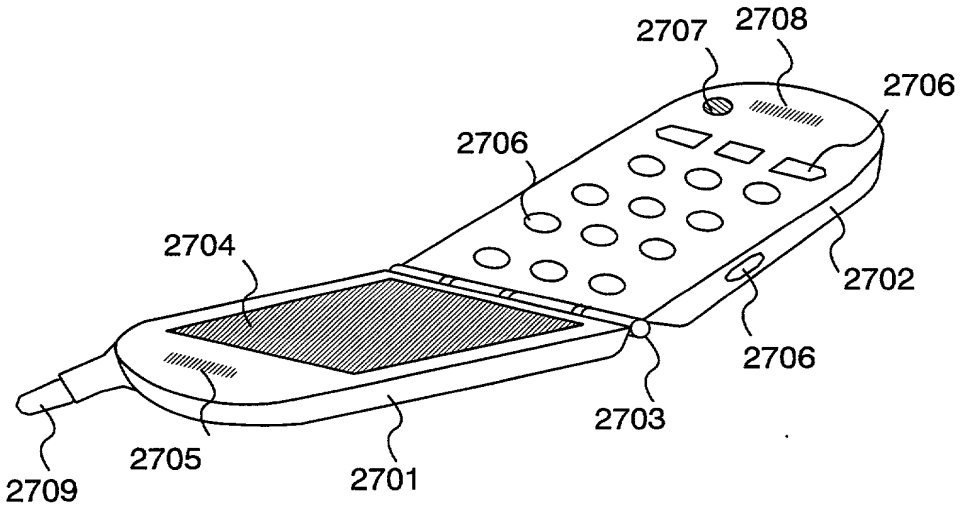


Fig. 31

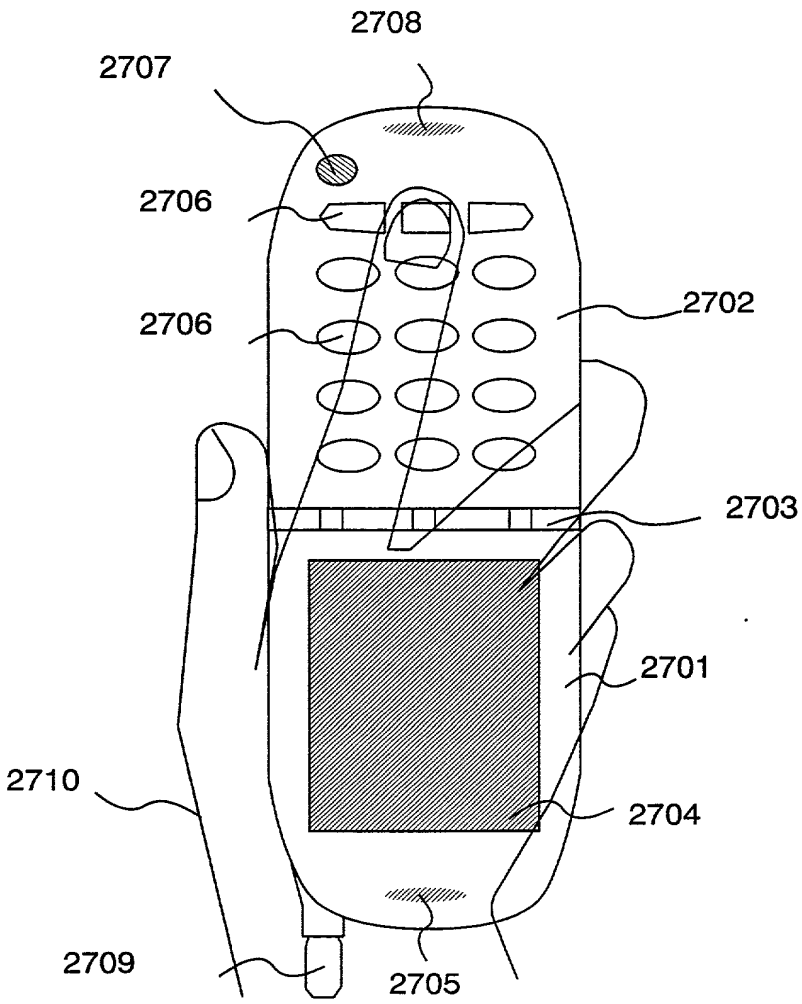


Fig. 32

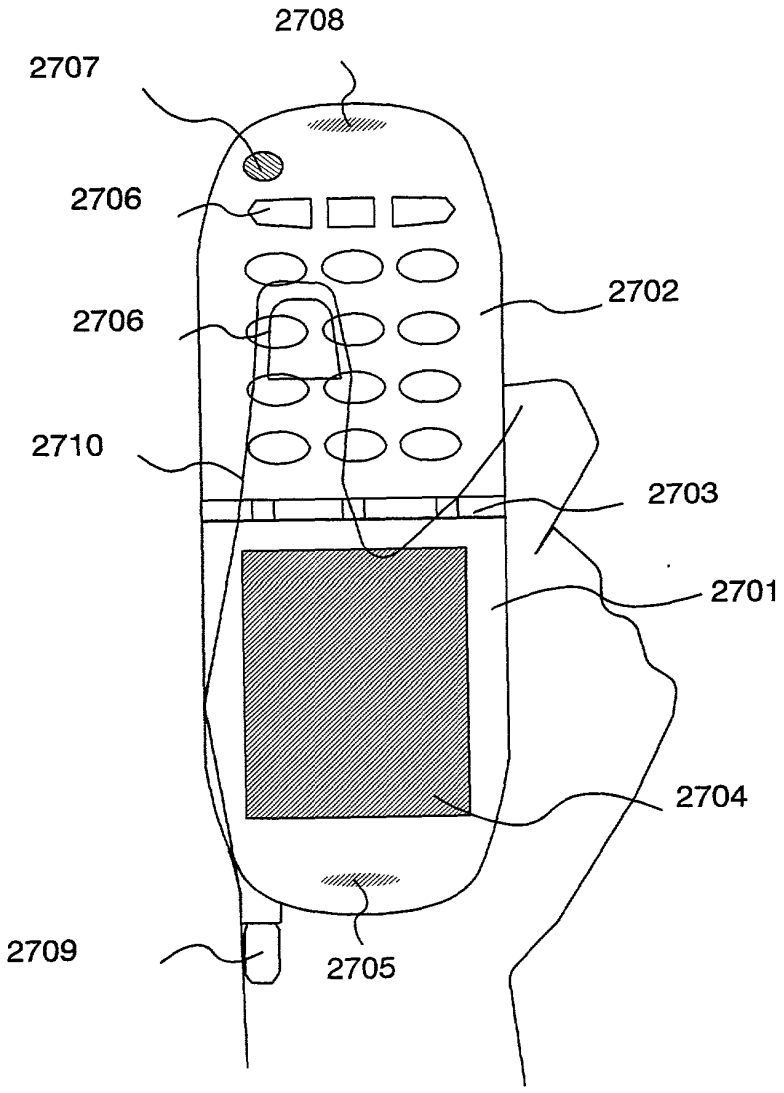


Fig. 33

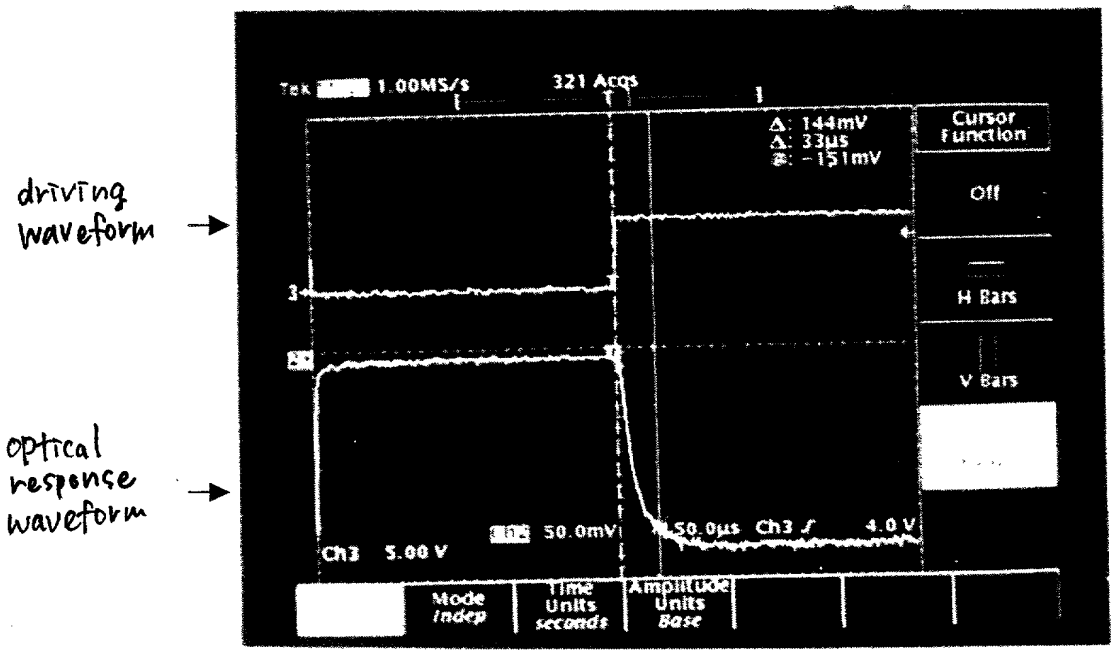

driving waveform
optical response waveform
Tek 1.00MS/s
321 Acqs
Δ: 144mV
Δ: 33µs
@: -151mV
Cursor Function
Off
H Bars
V Bars
Ch3 5.00 V
50.0mV
50.0µs Ch3 ƒ 4.0 V
Mode Indep
Time Units seconds
Amplitude Units Base

Fig. 34